## What is claimed is:

- 1. A memory device comprising:
  - a plurality of memory array blocks, each comprising a plurality of memory cells arranged in rows that are coupled together by wordlines; and a row decoder coupled to the plurality of memory array blocks through the wordlines.
- 2. The memory device of claim 1 and further including a plurality of external address signals coupled to the row decoder such that a wordline is selected in response to the address signals.
- 3. The memory device of claim 1 and further including a plurality of sense amplifiers coupled to outputs of the memory cells to detect data in the memory cells.
- 4. The memory device of claim 1 wherein each memory array block comprises 256 wordlines.
- 5. The memory device of claim 1 wherein the plurality of memory cells are flash memory cells.
- 6. The memory device of claim 1 wherein the memory device is a NAND flash memory device.
- 7. The memory device of claim 1 wherein the memory device is a NOR flash memory device.
- 8. The memory device of claim 1 wherein the plurality of memory array blocks comprises eight memory array blocks.

- 9. A flash memory device comprising:
  - a plurality of n-wells comprising an n-type conductivity material;
  - a plurality of p-wells comprising a p-type conductivity material, each p-well located within an n-well;
  - a plurality of flash memory array blocks, each comprising a plurality of flash memory cells arranged in rows that are coupled together by wordlines, each flash memory array block located within a different p-well of the plurality of p-wells; and
  - a row decoder coupled to the plurality of memory array blocks through the wordlines, external address signals coupled to the row decoder such that a wordline is selected in response to the address signals.
- 10. The flash memory device of claim 9 wherein a voltage of 0V is applied to the n-well and a voltage of -5V is applied to the p-well of an unselected flash memory array block during an erase operation.
- 11. The flash memory device of claim 9 wherein a voltage of 5V is applied to the n-well and a voltage of 5V is applied to the p-well of an unselected flash memory array block during a program operation.
- 12. A memory device comprising:
  - a plurality of memory array blocks arranged in rows comprising at least two
    memory array blocks, each memory array block comprising a plurality of
    memory cells arranged in rows that are coupled together by wordlines; and
    a plurality of row decoders, each row decoder coupled to a subset of the plurality of
    memory array blocks through the wordlines.
- 13. A flash memory device comprising:a plurality of lower wells comprising a first conductivity material;

- a plurality of isolation wells comprising a second conductivity material, each isolation well located within a lower well;
- a plurality of flash memory array blocks, each comprising a plurality of flash memory cells arranged in rows that are coupled together by wordlines, each flash memory array block located within a different isolation well of the plurality of isolation wells; and
- a row decoder coupled to the plurality of memory array blocks through the wordlines, external address signals coupled to the row decoder such that a wordline is selected in response to the address signals.
- 14. The flash memory device of claim 9 wherein a voltage of 0V is applied to the lower well and a voltage of -5V is applied to the isolation well of an unselected flash memory array block during an erase operation.
- 15. The flash memory device of claim 9 wherein a voltage of 5V is applied to the lower well and a voltage of 5V is applied to the isolation well of an unselected flash memory array block during a program operation.
- 16. The flash memory device of claim 9 wherein the first conductivity material is an n-type conductivity material.
- 17. The flash memory device of claim 9 wherein the second conductivity material is a p-type conductivity material.
- 18. A method for programming a memory cell in a memory array block of a plurality of memory array blocks, each memory array block located within a first conductivity material that is located within a second conductivity material, the method comprising:

generating an address signal of the memory cell;

- a row decoder selecting, in response to the address signal, a wordline signal that is coupled to the memory cell, the wordline signal additionally coupled to the plurality of memory array blocks;
- coupling a first voltage that is greater than 0V to the first conductivity material of memory array blocks that are not selected by the wordline signal; and coupling a second voltage that is greater than 0V to the second conductivity material of memory array blocks that are not selected by the wordline signal.
- 19. The method of claim 18 wherein the first and second voltages are substantially equal to +5V.
- 20. A method for erasing a memory cell in a memory array block of a plurality of memory array blocks, each memory array block located within a first conductivity material that is located within a second conductivity material, the method comprising:

generating an address signal of the memory cell;

- a row decoder selecting, in response to the address signal, a wordline signal that is coupled to the memory cell, the wordline signal additionally coupled to the plurality of memory array blocks; and
- coupling a voltage that is less than 0V to the second conductivity material of memory array blocks that are not selected by the wordline signal.
- 21. The method of claim 20 wherein the voltage is substantially equal to -5V.
- 22. An electronic system comprising:
  - a processor that controls operation of the electronic system and generates address signals; and
  - a flash memory device coupled to the processor, the device comprising:

a plurality of memory array blocks, each comprising a plurality of memory cells arranged in rows that are coupled together by wordlines; and a row decoder coupled to the plurality of memory array blocks through the wordlines, the row decoder coupled to the address signals and selecting a wordline in response to the address signals.